Ser. No. 10/775,468
Internal Docket No. PD030016
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Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) Method for pre-processing input signals of interfaces of different type for common-format central processing, using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said method including the steps:

- generating from the ~~different-type interface~~ input signals of interfaces of different type system clock synchronised input signals;
- channel decoding said system clock synchronised input signals according to [[the]] differing channel protocols related to said different-type interfaces, thereby providing corresponding PCM bitstream format signals having a uniform word format;
- further processing said PCM bitstream format signals so as to form therefrom sample words that are stored in an intermediate store~~, e.g. a FIFO,~~ from which the sample words are fed to said central processing.

2. (Currently amended) Method for pre-processing output signals for interfaces of different type in a common-format central processing using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said method including the steps:

- further processing sample words that were output from said central processing and stored in an intermediate store~~, e.g. a FIFO,~~ by forming system clock synchronised PCM bitstream format signals therefrom, which PCM bitstream format signals have a uniform word format and are related to said interfaces of different type;
- channel encoding said system clock synchronised PCM bitstream format signals having a uniform word format according to [[the]] differing channel

protocols related to said different-type interfaces, thereby providing corresponding system clock synchronised output signals;

- generating from said system clock synchronised output signals interface-type related output signals ~~(SADO)~~ that are no more system clock synchronised but conform to said type of interface.

3. (Currently amended) Apparatus for pre-processing input signals of interfaces of different type for common-format central processing, using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said apparatus including:

- means for generating from the ~~different-type interface~~ input signals of interfaces of different type system clock synchronised input signals;
- means for channel decoding said system clock synchronised input signals according to [[the]] differing channel protocols related to said different-type interfaces, thereby providing corresponding PCM bitstream format signals having a uniform word format;
- means for further processing said PCM bitstream format signals so as to form therefrom sample words that are stored in an intermediate store~~, e.g. a FIFO,~~ from which the sample words are fed to a central processing.

4. (Currently amended) Apparatus for pre-processing output signals for interfaces of different type in a common-format central processing using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said apparatus including:

- means for further processing sample words that were output from said central processing and stored in an intermediate store~~, e.g. a FIFO,~~ by forming system clock synchronised PCM bitstream format signals therefrom, which PCM bitstream format signals have a uniform word format and are related to said interfaces of different type;
- means for channel encoding said system clock synchronised PCM bitstream format signals having a uniform word format according to [[the]] differing

channel protocols related to said different-type interfaces, thereby providing corresponding system clock synchronised output signals;

- means for generating from said system clock synchronised output signals interface-type related output signals that are no more system clock synchronised but conform to said type of interface.

5. (Previously Presented) Method according to claim 1, wherein said interface types include at least two of IEC958, I2S, AC-Link and ADAT.

6. (Currently amended) Method according to claim 1, wherein some individual samples are marked or checked with their channel type in the system clock synchronised processing in order to detect and avoid channel permutation, said channel permutation occurring [[e.g.]] in case of insertion or deletion of samples, said marking being carried out [[e.g.]] by using subcode bits that are otherwise not used in said system clock synchronised processing.

7. (Previously Presented) Method according to claim 1, wherein for DMA data block transfer in connection with said intermediate storage an LF marking is carried out for the first word of each DMA data block and is evaluated in order to reduce the number of processor operations when preparing a DMA buffer output.

8. (Previously Presented) Method according to claim 1, wherein for facilitating a precisely timed start-up of a stream unit that performs said further processing of the sample words, an internally generated time stamp is supplied to the stream unit by the central processing.

9. (Currently amended) Method according to one of ~~claims~~ claim 1, wherein for synchronisation of interface signals that have separate clock and data or sync signals to said system clock, two succeeding D flip-flops are used that are clocked by the same edge of the clock to be synchronised.

10. (Previously Presented) Apparatus according to claim 3, wherein said interface types include at least two of IEC958, I2S, AC-Link and ADAT.

11. (Currently amended) Apparatus according to claim 3, wherein some individual samples are marked or checked with their channel type in the system clock synchronised processing in order to detect and avoid channel permutation, said channel permutation occurring [[e.g.]] in case of insertion or deletion of samples, said marking being carried out [[e.g.]] by using subcode bits that are otherwise not used in said system clock synchronised processing.

12. (Previously Presented) Apparatus according to claim 3, wherein for DMA data block transfer in connection with said intermediate storage an LF marking is carried out for the first word of each DMA data block and is evaluated in order to reduce the number of processor operations when preparing a DMA buffer output.

13. (Previously Presented) Apparatus according to claim 3, wherein for facilitating a precisely timed start-up of a stream unit that performs said further processing of the sample words, an internally generated time stamp is supplied to the stream unit by the central processing.

14. (Previously Presented) Apparatus according to claim 3, wherein for synchronisation of interface signals that have separate clock and data or sync signals to said system clock, two succeeding D flip-flops are used that are clocked by the same edge of the clock to be synchronised.

15. (New) The method according to claim 1, wherein the intermediate store comprises a FIFO.

16. (New) The method according to claim 2, wherein the intermediate store comprises a FIFO.

17. (New) The apparatus according to claim 3, wherein the intermediate store comprises a FIFO.

18. (New) The apparatus according to claim 4, wherein the intermediate store comprises a FIFO.